

LC7537, 7537AN, 7537NE

Electronic Volume Control System for Audio Equipment

Overview

The LC7537N is an electronic control LSI capable of electronically controlling the volume, balance, loudness, fader, bass, and treble functions individually with fewer externally connected component parts.

Features

- Enables controlling the below-listed functions with 3line serial data, including CE, DI, and CLK. Also, due to 0 V to 5 V swing of the serial data input voltage, permits the use of a general purpose microcomputer.
 - Volume : Separately controls the Lch and Rch volume levels across 81 positions over the 0 dB to −79 dB (in 1 dB steps) range and -∞, and consequently also serves balance control purposes.
 - Loudness : By virtue of a center tap provided at the -20 dB position of the volume controlling ladder resistors, permits loudness to be controlled with externally connected CR components.
 - Fader : By varying only the rear or front output level across 16 positions, provides fader functions (in 2 dB steps over the 0 dB to -20 dB range, and 5 dB steps over the -20 dB to -45 dB range, and at -∞, for a total of 16 positions).
 - Bass/Treble: With CR components externally connected, forms an NF type tone control circuit (Baxandall type) to exercise control across 15 positions over both the bass and treble functions in 2 dB steps.
- By virtue of its CMOS structure, the LSI operates under a broad power supply voltage range from +4.5 V to +15 V, permitting the use of either a single or a dual ± power supply, whichever is preferred.

Package Dimensions

unit : mm **3025B-DIP42S**



unit : mm

3052A-QFP48A



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Pin Assignments



Equivalent Circuit Block Diagram



Specifications

VDD VCC VEE VSS

Absolute Maximum Ratings at Ta = 25°C, $V_{SS} = 0 V$, $V_{DD} = \ge V_{CC} > V_{SS} \ge V_{EE}$

| Item | Symbol | Condition | Rating | Unit |
|-------------------------------|---------------------------------------|---|----------------------------------|------|
| | V _{DD} – V _{EE} max | V_{DD} , V_{EE} : $V_{EE} \ge -8 V$ | 16 | V |
| Maximum supply voltage | V _{CC} max | V_{CC} : $V_{DD} \ge V_{CC}$ | V_{SS} – 0.3 to V_{SS} + 7 | V |
| land the second second second | V _{I1} | DI, CLK, CE | $V_{SS} - 0.3$ to V_{DD} + 0.3 | V |
| Input supply voltage | V _{I2} | ĪNIT | $V_{SS} - 0.3$ to V_{DD} + 0.3 | V |
| | Del marci | Ta ≤ 85°C, (LC7537N, 7537AN) | 200 | mW |
| Allowable power dissipation | Pd max | Ta ≤ 85°C, (LC7537NE) | 300 | mW |
| Operating temperature | Topr | | -40 to +85 | °C |
| Storage temperature | Tstg *3 | | -50 to +125 | °C |

Allowable Operating Conditions at Ta = 25°C, $V_{SS} = 0 V$, $V_{DD} = \geq V_{CC} > V_{SS} \geq V_{EE}$

| Item | Symbol | Condition | Rating | Unit |
|--------------------------|----------------------------------|-----------------------------|--|------------------|
| Quantum the new Wd | V _{DD} -V _{EE} | $V_{EE} \ge -7.5 \text{ V}$ | 4.5 to 15 | V |
| Supply voltage *1 | V _{CC} | | 4.5 to 5.5 | V |
| | V _{IH1} *2 | DI, CLK, CE | 0.8 V _{CC} to V _{CC} | V |
| Input nign-level voltage | V _{IH2} | ĪNIT | 0.8 ($V_{DD} - V_{EE}$) + V_{EE} to V_{DD} | V |
| | V _{IL1} *2 | DI, CLK, CE | V_{SS} to 0.2 V_{CC} | V |
| Input low-level voltage | V _{IL2} | ĪNIT | V_{EE} to 0.2 ($V_{DD} - V_{EE}$) + V_{EE} | V |
| Input signal amplitude | V _{IN} | | V _{EE} to V _{DD} | V _{P-P} |
| Input pulse width | tø _W | | 1 min | μs |
| setup time | t _{set up} | | 1 min | μs |
| Hold time | t _{hold} | | 1 min | μs |
| Operating frequency | f _{opg} | | up to 330 | kHz |

Note: 1. A1000 pF or larger capacitor should be added on between each individual power supply terminal and V_{SS}.

2. When the microcomputer side control signals rise faster than V_{DD} for the LC7537, a 2 kΩ or higher resistor should be inserted midway on each of the DI, CLK, and CE lines

3. When mounting the QIP package on the board, do not dip the entire package in solder. Only the LC7537NE may be dipped directly in solder during mounting.

| Electrical Characteristics at Ta = 25°C | , V _{DD} =+7.5 V, V | $V_{\rm EE} = -7.5 \rm V, V_{\rm CC} = +5 \rm V$ |
|---|------------------------------|---|
|---|------------------------------|---|

| Itom | Symbol | Symbol Condition | | Rating | | | |
|----------------------------|-----------------------|--|-------|--------|------|------|--|
| nem | Symbol | | | typ | max | Unit | |
| Total harmonic | THD(1) | V _{IN} = 1 V, f = 1kHz, all flat overall | | 0.005 | 0.01 | % | |
| Distortion | THD(2) | V _{IN} = 1 V, f = 20 kHZ, all flat overall | 0.006 | 0.02 | % | | |
| | СТ | $V_{IN} = 1 \text{ V}, \text{ f} = 1 \text{ kHz}, \text{ all flat, } \text{Rg} = 1 \text{ k}\Omega$ | 60 | 95 | | dB | |
| Crosstalk | V _{omin} (1) | V_{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞ , FADER VR = ∞ | 80 | 90 | dB | | |
| Maximum attenuation output | V _{omin} (2) | V_{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞ , V_{DD} = 8 V, FADER VR = ∞ , V_{EE} = V_{SS} = 0 V, C between V_{SS} and GND of L/R = 1000 μ F | 70 | 80 | | dB | |
| | R _{VOL} (1) | 5 dB-step | 12 | 20 | 28 | kΩ | |
| | R _{VOL} (2) | 1 dB-step | 12 | 20 | 28 | kΩ | |
| VR resistance voltage | R _{BASS} | | 12 | 20 | 28 | kΩ | |
| | R _{TREBLE} | | 12 | 20 | 28 | kΩ | |
| | R _{FADER} | | 12 | 20 | 28 | kΩ | |
| | V _N (1) | All flat overall (I _{HF-A}) Rg = 1 k Ω | | 2 | 10 | μV | |
| Output hoise | V _N (2) | $Rg = 1 k\Omega$, $V_{DD} = 8 V$, $V_{EE} = V_{SS} = 0 V$ | | 2 | 10 | μV | |
| Oursent design | I _{DD} | $V_{DD} - V_{EE} = 15 V$ | | | 1 | mA | |
| | I _{CC} | V _{CC} = 5 V | | | 1 | mA | |

Pin Description (): LC7537AN, 7537NE

| 12(8) LIN Main volume control block 5 dB-step attenuator input terminals. These pins should be 9(4) LC1 Main volume control block 5 dB-step attenuator output terminals. Having been designed VR resistance : 20 KΩ 9(4) LC2 Main volume control block 1 dB-step attenuator input terminals. These pins should be VR resistance : 20 KΩ 10(5) LC2 Main volume control block 1 dB-step attenuator input terminals. These pins should be provided. VR resistance : 20 KΩ 11(6) LOUT Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, load impedances as high a possible should be provided to provided to provided to provided to the step ositions designed to be open, load impedances as high a possible should be provided to provided to provided to the step ositions designed to be open, load impedances do Lok will be the same as on RD, bud be provided to them. VR resistance : 20 kΩ 63(3) R.FIN Fader functions employing mode input terminals. These pins should be driven at a low predendenty of each other. Attenuations exercised on Lok will be the same as on RD, bud be provided to them. VR resistance : 20 kΩ 63(3) R.ROUT Fader functions edsigned to be open, acceptor impedances as high a possible should be fraven at a side be faded out, bud the step ositions designed to the open, acceptor impedances as high as possible and provided in 2 dB step VR resistance : 20 kΩ 11(10) LB2 Bass tone control | Pin No. | Symbol | Description of Functions | Remarks | |
|---|---------|--------|---|-------------------------------|--|
| 31(29) R.N driven at a low impedance. 9(4) LC1 Main volume control block 5 dB-step attenuator output terminals. Having ben designed big hoad impedances as possible should be provided. WR resistance : 20 kΩ 34(30) RC1 Main volume control block 1 dB-step attenuator input terminals. Theses pins should be driven at alow impedance. WR resistance : 20 kΩ 10(6) LC2 Main volume control block 1 dB-step attenuator input terminals. Theses pins should be provided. WR resistance : 20 kΩ 3(3) R.OUT Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, local impedances as high as possible should be provided to provided to the m, similar to those for the LC1 and RC1. 3(4) R.OUT Fader block output terminals. These pins should be driven at a low independently of each other. Attenuations exercised on Lch will be the same as on Rch, should be provided to the m. VR resistance : 20 kΩ 3(4) LROUT Fader block output terminals. A total of 15 positions have been provided in 2 dB steps VR resistance : 20 kΩ 3(4) LROU Bass to ne control block terminals. A total of 15 positions have been provided in 2 dB steps. VR resistance : 20 kΩ 3(4) LROUT Fader block control block terminals. A total of 15 positions have been provided in 2 dB steps. VR resistance : 20 kΩ 3(4) LROUT Fader block control block terminals. A total of 15 positions have been provided in 2 dB steps. <t< td=""><td>12(8)</td><td>L.IN</td><td>Main volume control block 5 dB-step attenuator input terminals. These pins should be</td><td></td></t<> | 12(8) | L.IN | Main volume control block 5 dB-step attenuator input terminals. These pins should be | | |
| 9(4) LC1 Main volume control block 5 dB-step attenuator output terminals. Having been designed to be open, the step positions will develop errors if at low acceptor impedances, so that as high load impedances as possible should be provided. VR resistance : 20 kΩ 10(5) LC2 Main volume control block 1 dB-step attenuator input terminals. Theses pins should be driven at alow impedance. VR resistance : 20 kΩ 11(6) LOUT Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, load impedances as high as possible should be provided to triven at alow impedance. VR resistance : 20 kΩ 32(31) R.OUT Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, load impedances as high as possible should be provided to triven, similar to those for the LC1 and RC1. VR resistance : 20 kΩ 33(30) R.FIN impedance. VR resistance : 20 kΩ 34(40) LFOUT Fader functions employing mode input terminals. These pins should be driven at a low independently of each other. Attenuations exercised on Lch will be the same as on Rch. Due to the step positions designed to be open, acceptor impedances as high as possible should be provided to therm. VR resistance : 20 kΩ 11(1) LB1 Bass tone control block terminals. A total of 15 positions have been provided in 2 dB steps VR resistance : 20 kΩ 27(28) R.12 | 31(29) | R.IN | driven at a low impedance. | | |
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| 40(40)R.ROUTShould be provided to them.15(11)L.B116(9)L.B214(10)L.B328(26)R.B127(28)R.B229(27)R.B317(13)L.T116(12)L.T218(14)L.T326(24)R.T125(23)R.T27(1)LCT140(4)L.C137(1)LCT16(48)LCT26(48)LCT26(48)LCT236(36)RCT137(37)RCT2 | 39(39) | R.ROUT | Due to the step positions designed to be open, acceptor impedances as high as possible | | |
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| 16(9)L.B2Bass tone control block terminals. A total of 15 positions have been provided in 2 dBVR resistance : 20 kΩ28(26)R.B1steps27(28)R.B229(27)R.B317(13)L.T116(12)L.T218(14)L.T326(24)R.T125(23)R.T225(23)R.T37(1)LCT16(48)LCT26(48)LCT26(48)LCT258(36)RCT17(17)LCT258(36)RCT17(17)LCT258(36)RCT17(17)LCT258(36)RCT17(17)LCT258(36)RCT17(17)LCT258(36)RCT17(17)LCT27(17)LCT27(17)LCT27(17)LCT27(18)LCT27(19)LCT27(17)LCT27(18)LCT27(19)LCT27(17)LCT27(17)LCT27(18)Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-VS S7(17)RCT2 | 15(11) | L.B1 | | | |
| 14(10)L.B3 RB1Bass tone control block terminals. A total of 15 positions have been provided in 2 dB stepsVR resistance : 20 kΩ28(26)R.B1 | 16(9) | L.B2 | | | |
| 28(26)R.B1steps27(28)R.B229(27)R.B317(13)L.T116(12)L.T218(14)L.T318(14)L.T326(24)R.T1steps. The VR resistance value is 20 kΩ.27(25)R.T225(23)R.T37(1)LCT16(48)LCT26(48)LCT26(48)LCT236(36)RCT137(37)RCT2 | 14(10) | L.B3 | Bass tone control block terminals. A total of 15 positions have been provided in 2 dB | VR resistance : 20 kΩ | |
| 27(28)R.B2R.B229(27)R.B317(13)L.T116(12)L.T218(14)L.T326(24)R.T126(24)R.T1steps. The VR resistance value is 20 kΩ.27(25)R.T225(23)R.T37(1)LCT16(48)LCT2between CT1 and IN, and low-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS}).37(37)RCT2 | 28(26) | R.B1 | steps | | |
| 29(27)R.B3Image: Relation of the second seco | 27(28) | R.B2 | | | |
| $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | 29(27) | R.B3 | | | |
| 16(12)L.T2L.T3Treble tone control block terminals. A total of 15 positions have been provided in 2 dBVR resistance : 20 kΩ18(14)L.T3Treble tone control block terminals. A total of 15 positions have been provided in 2 dBVR resistance : 20 kΩ26(24)R.T4Freble tone control block terminals. A total of 15 positions have been provided in 2 dBVR resistance : 20 kΩ27(25)R.T2Freble tone control block terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS} VR resistance : 20 kΩ37(37)RCT2KCT1KCT2Loudness dedicated terminals. A high-frequency-range correcting C between CT2 and L-V _{SS} | 17(13) | L.T1 | | | |
| 18(14)L.T3 R.T4Treble tone control block terminals. A total of 15 positions have been provided in 2 dB steps. The VR resistance value is 20 kΩ.VR resistance : 20 kΩ27(25)R.T2 | 16(12) | L.T2 | | | |
| 26(24) R.T1 steps. The VR resistance value is 20 kΩ. VR resistance . 20 K2 27(25) R.T2 25(23) R.T3 7(1) LCT1 Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L ⁻ V _{SS}). VR resistance . 20 K2 36(36) RCT1 (R-V _{SS}). | 18(14) | L.T3 | Treble tone control block terminals A total of 15 positions have been provided in 2 dB | VB registered : 20 kG | |
| 27(25) R.T2 25(23) R.T3 7(1) LCT1 6(48) LCT2 between CT1 and IN, and low-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS} 37(37) RCT2 | 26(24) | R.T1 | steps. The VR resistance value is 20 k Ω . | | |
| 25(23) R.T3 7(1) LCT1 6(48) LCT2 36(36) RCT1 37(37) RCT2 | 27(25) | R.T2 | | | |
| 7(1) LCT1 6(48) LCT2 36(36) RCT1 37(37) RCT2 Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS} | 25(23) | R.T3 | | | |
| 6(48) LCT2 Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L-V _{SS} (R-V _{SS}). 37(37) RCT2 | 7(1) | LCT1 | | | |
| 36(36) RCT1 between CT1 and inv, and low-nequency-range correcting C between CT2 and L=V _{SS} 37(37) RCT2 | 6(48) | LCT2 | Loudness dedicated terminals. A high-frequency-range correcting C should be put | | |
| 37(37) RCT2 | 36(36) | RCT1 | $(R-V_{SS})$. | | |
| | 37(37) | RCT2 | | | |

Continued on next page.

LC7537N, 7537AN, 7537NE

Continued from preceding page.

| Pin No. | Symbol | Description of Functions | Remarks | |
|--------------------------------------|--|--|-------------------------------|--|
| 8(2) | L-V _{SS} | Main volume control block fader control common terminals. The impedance of pattern connected to these pins should be as low as possible. Since $L-V_{SS}$ ($R-V_{SS}$) and V_{SS} have not been connected inside the LSI, they should be connected together on the outside in conformance with their individual specifications. Particular attenuation should be paid to the capacitance assigned to the capacitors put between $L-V_{SS}$ ($R-V_{SS}$) and V_{SS} , which will emerge as a residual resistive component when control is turned down for maximum | | |
| 35(35) | R-V _{SS} | attenuation. | | |
| 42(42) | INIT | Intra-IC latch resetting terminal INIT CE Control-setting data at the internal latch will be indeterminate when power has just been switched on, so that by engaging the "L" level of this pin at power-on, the fader control may be set at its — position and muting behaviour is engaged (Note: V _{DD} to V _{EE} Level). | | |
| 22(20) | CE | Chip enable terminal. When this pin is made "H" to "L", data is written in the internal latch, activating the various analog switches. When the "H" level is then restored, transfer of the data will be enabled. | CE WCC | |
| 20(16) | DI | Input terminals for serial data and clock that serve control nurnoses | | |
| 21(17) | CLK | | y Vss | |
| 1(43) 23(21) 19(15) 24(22) | V _{DD} V _{CC} V _{SS} V _{EE} | These pins are connected to the relevant power supplies. Exercise caution against $V_{\mbox{CC}}$ rising earlier than $V_{\mbox{DD}}$ | | |
| 2(3, 7) 41(18, 30, 34, 41, 44) | NC | No connect pins. Absolutely nothing should be connected here. | | |
| (19) | V _{DD} (NC) | V _{DD} subterminal. Connected to V _{DD} or left open. | LC7537AN and LC7537NE only | |

Control Timing



Data Format







Fader Volume Control Block Equivalent Circuit







Rch is similarly structured.

Sample Application Circuits

Single Power Supply



Unit (resistance: Ω, capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

Dual ± Power Supply



Unit (resistance: Ω, capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

Single Power Supply



Unit (resistance: Ω , capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.





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